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| 09/813,973 | 03/22/2001 | Hideyuki Toriyama | 245402002600 | 6050 |

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| EXAMINER | |
|---|---|
| CARTER, TIA A | |
| ART UNIT | PAPER NUMBER |
| 2626 | |

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/813,973 | TORIYAMA, HIDEYUKI | |
| | Examiner | Art Unit | |
| | Tia A Carter | 2626 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3-22-2001.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-4, 12-26, and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 1: a memory device provided at a preceding stage of said first processing means to store said pixel data. The "memory device" disclosed is not supported by the specification on page 9, lines 22-24.

Regarding claim 2: "a connecting means for " is not supported in specification as cited on page 10, lines 5-6.

Regarding claim 3: a connecting means for " is not supported in specification as cited on page 10, lines 5-6.

"a switch device for arranging a plurality of said connecting means, corresponding to said plurality of color data, at a preceding stage of said first processing means in said first state, and for arranging said connecting means, corresponding to said one image color data, between said first processing means and said second processing means in said second state" is not supported in specification as cited on page 10, lines 13-29.

Regarding claim 4: a memory device to store said pixel data. The "memory device" disclosed is not supported by the specification as cited on page 9, lines 22-24.

Regarding claim 12: the limitation is not supported by the specification at all:

Said third processing unit substantially simultaneously receives the image data from said first processing unit and data corresponding to said image data from said second processing unit.

Regarding claim 13: these limitations are not supported by the specifications as cited on page 10, lines 3-4:

A first circuit to input the image data output from said memory device into said first processing unit.

A second circuit to input the image data output from said first processing circuit unit into said memory device and also to input the image data output from said memory device into said second processing unit.

A switch device to selectively switch said first circuit and said second circuit.

Regarding claim 20: these limitations are not supported by the specification as cited on page 10, lines 3-4:

a first circuit to input image data including a set of a plurality of color data output from said memory device into said first processing unit;

a second circuit to input one image color data output from said first processing unit into said memory device, and also inputting one image color data output from said memory device into said second processing unit; and

a switch device to selectively switch said first circuit and said second circuit to select said first circuit in said first state and to select said second circuit in said second state.

Regarding claim 28: these limitations are not supported by the specification as cited on page 10, lines 3-4:

a first circuit to input image data including a set of a plurality of color data output from said memory device into said first processing unit;

a second circuit to input one image color data output from said first processing unit into said memory device, and also inputting one image color data output from said memory device into said second processing unit; and

a switch device to selectively switch said first circuit and said second circuit.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-11 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida et al. (US. 6538769).

Regarding claim 1, Yoshida discloses an image processing apparatus (fig. 1, col. 2, lines 49-51), comprising:

a first processing means for (HVC-125) sequentially processing input pixel data (fig. 2 col. 4, lines 41-46 and col. 5, lines 18-26);

a memory device (internal memory of connection unit 123) provided at a preceding stage of said first processing means to store said pixel data (fig. 2, col. 4, lines 14-19);

a second processing means for (area discrimination 144) determining a characteristic of an image region including a plurality of said pixel data (fig. 2, col. 5, lines 37-46); and

a third processing means for (MTF 136) processing the pixel data processed at said first processing means, based on the characteristic determined by said second processing means (fig.2, col. 5, lines 46-51).

Regarding claim 2, Yoshida disclose an image processing apparatus (fig. 1, col. 2, lines 49-51), comprising:

a first processing means for (HVC 125) sequentially processing pixel data in response to input of the pixel data (fig. 2, col. 4, lines 41-46 and col. 5, lines 18-26);

a second processing means for (area discrimination 144) determining a characteristic of an image region including a plurality of said pixel data (fig.2, col. 5, lines 37-46);

a third processing means for (MTF 136) processing pixel data processes at said first processing means, based on the characteristic determined by said second processing means fig.2, col. 5, lines 47-52);

a connecting means (selector 112/113) for connecting a memory device (126); and

a switch device (selector 112 /113) for switching a circuit such that said connecting means is arranged either at a preceding stage of said first processing means or between said first processing means and said third processing means (see figure. 2). As disclosed in the specification on page 10, lines 5-33, figure 2, the applicant cites connecting relationships between the switches (selector) and the processing units. Also, cited on page 11, a line 4-8, the applicants clearly establishes a

relationship between the connecting means and the switch as being a combined function.

Regarding claim 3, Yoshida disclose an image processing apparatus (fig. 1, col. 2, lines 49-51), comprising;

a first processing means for (HVC-125) converting, in response to input of pixel data including a set of a plurality of color data, said plurality of color data into a plurality of image color data in a first state, and said plurality of color data into one image color data of said plurality of image color data in a second state (fig. 2, col. 4, lines 41-46 and col. 5, lines 18-26);

a second processing means for (area discriminating 144) determining a characteristic of an image region including a plurality of said pixel data (fig. 2, col. 5, lines 37-46);

a third processing means for (MTF 136) processing, based on a characteristic amount determined by said second processing means, said plurality of image color data converted at said first processing means in said first state, and the one image color data converted at said first processing means in said second state (fig.2, col. 5, lines 47-52);

a connecting means for (selector 112/113) connecting a memory device (126); and

a switch device for (selector 112/113) arranging a plurality of said connecting means, corresponding to said plurality of color data, at a preceding stage of said first processing means in said first state, and for arranging said connecting means, corresponding to said one image color data, between said first processing means and

said second processing means in said second state (see figure 2). ). As disclosed in the specification on page 10, lines 5-33, figure 2, the applicant cites connecting relationships between the switches (selector) and the processing units. Also, cited on page 11, a line 4-8, the applicants clearly establishes a relationship between the connecting means and the switch as being a combined function.

Regarding claim 4, Yoshida disclose an image processing apparatus (fig. 1, col. 2, lines 49-51), comprising:

a memory device (123) to store input image data (fig. 2, col. 4, lines 14-19);

a first processing unit (HVC 125) to sequentially convert and output the image data stored in said memory device (fig. 2, col. 4, lines 41-46 and col. 5, lines 18-26);

a second processing unit (144) to receive the same image data as image data input into said memory device and to output data processed based on the received image data (fig.2, col. 5, lines 37-46); and

a third processing unit (MTF 136) to receive the image data output from said first processing unit and the data output from said second processing unit, and to process the image data output from said first processing unit based on the data output from said second processing unit (fig. 2, col. 5,lines 46-51).

Regarding claim 5, Yoshida et al. discloses the image processing apparatus according to claim 4, wherein same image data is input into said memory device and said second processing unit in parallel (see figure 2).

Regarding claim 6, Yoshida et al. discloses the image processing apparatus according to claim 4, wherein said second processing unit determines an attribute of an image 5 region based on image data of a pixel to be processed and pixels on the periphery of said pixel to be processed, and outputs data indicating the attribute (fig. 2, col. 5, lines 38-46).

Regarding claim 7, Yoshida et al. discloses the image processing apparatus according to claim 6, wherein said second processing unit determines if the image region is represented by a character (fig. 2, col. 5, lines 38-46).

Regarding claim 8, Yoshida et al. discloses the image processing apparatus according to claim 6, wherein said second processing unit determines if the image region is represented by a photograph (fig. 2, col. 5, lines 38-46).

Regarding claim 9, Yoshida et al. discloses the image processing apparatus according to claim 6, wherein said second processing unit determines if the image region is represented by a dot (fig. 2, col. 5, lines 38-46).

Regarding claim 10, Yoshida et al. discloses the image processing apparatus according to claim 4, wherein said first processing unit converts the input image data into image data of a different color system to output the converted image data (fig. 2, col. 4, lines 41-46).

Regarding claim 11, Yoshida et al. disclose the image processing apparatus according to claim 4, wherein said third processing unit processes the image data output from said first processing unit to correct sharpness of an image (fig. 2, col. 5,lines 47-50).

Regarding claim 27, Yoshida disclose an image processing apparatus (fig. 1, col. 2, lines 49-51), comprising:

a memory device (123) to store input image data (fig. 2, col. 4, lines 14-19);

a first processing unit (HVC 125) to sequentially convert and output the image data stored in said memory device (fig. 2, col. 4, lines 41-46 and col. 5, lines 18-26);

a second processing unit (144) to receive the same image data as image data input into said memory device and to output data processed based on the received image data (fig. 2, col. 5, lines 37-46); and

a third processing unit (MTF 136) to receive the image data output from said first processing unit and the data output from said second processing unit, and to process the image data output from said first processing unit based on the data output from said second processing unit (fig. 2, col. 5,lines 46-51).

An image-forming unit to form an image on a sheet based on image data output from said third processing unit (see figure 2).

***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hayashi et al. (US 2001/0048530) and Ikeda et al. (US. 6535302) are cited to show related art with respect to image processing in copying machines.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tia A Carter whose telephone number is 703 - 306-5433. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly A Williams can be reached on 703-305-4863. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tia A Carter
Examiner
Art Unit 2626

TAC
11/29/04

KIMBERLY WILLIAMS
SUPERVISORY PATENT EXAMINER